A Low-Power Multifunctional CMOS Sensor Node for an Electronic Facade

Xilin Liu, *Student Member, IEEE*, Milin Zhang, *Member, IEEE*, and Jan Van der Spiegel, *Fellow, IEEE*

***Abstract*—In this paper, a low-power, multifunctional CMOS smart sensor node is designed for an electronic facade, which provides an alternative solution to the concept of energy-efficient responsive buildings. Various sensing capabilities, including light intensity sensing, temperature sensing, motion tracking, and compressive image acquisition, are implemented on the sensor node. An 80×80 image pixel array is employed for motion tracking and compressive image acquisition. Various operational modes are realized, including: 1) event generation mode; 2) motion tracking mode; and 3) video output mode in full-resolution or compressed by the region of interest (ROI). A low-power, high-throughput motion detection algorithm is proposed in this paper. The power consumption of the proposed work is modeled, analyzed, and compared with traditional motion detection methods. According to numerical analysis, the throughput can be increased by 45% while using the proposed design instead of traditional temporal differential motion tracking methods with similar power consumption. The proposed algorithm is realized by a pixel-level focal-plane motion detection unit, consisting of switched-capacitor circuit, analog memory, and dual-threshold comparator. The proposed design was fabricated in 0.5 μm 3M2P standard CMOS technology, occupying 3×3 mm^2 silicon area. The total power consumption is 17 μW, while the pixel array is performing motion tracking with a frame rate of 30 fps and a supply voltage of 3.3 V.**

***Index Terms*—CMOS image sensor, compressive image acquisition, energy efficiency facade, focal plane processing, low-power motion detection, multifunctional sensor.**

I. Introduction

ACCORDING to reports from the U.S. Department of Energy, residential and commercial buildings consume nearly 40% of the total national energy [1]. Therefore, the design and production of new energy-efficient technologies are crucial to meet goals such as the Zero-Net Energy (ZNE) Building.

Traditional responsive architectural designs [2]–[7] rely heavily upon the use of bulky and power-hungry mechanically driven units, which are nested within a building facade system. Recent research explores the potential of electronic responsive material for building energy-efficient facades [8], [9]. Electronic devices are employed for the detection and/or monitoring of environmental changes, which are later used for the control of the responsive material. Since space heating, cooling, and lighting in buildings consume about 45.1% of the total building energy [1], it is crucial to monitor the building temperature and light intensity in an energy-efficient building design. In addition, motion detection enables a fast and accurate prediction of the rapid environmental changes that impact power consumption. In this paper, a smart sensor node that enables light intensity and temperature sensing, motion tracking and compressive image acquisition is described. This sensor has been employed for the control of self-assembled iron oxide colloidal particles [10], [11] filled in between two ITO glass to illustrate the concept of a responsive facade. Considering the scale of the building facades, the total number of the required distributed sensor nodes will be large. Thus the performance, power consumption, implementation cost, size, and robustness place a great challenge in the design of such a sensor node. Since CMOS technology enables an integration of various sensing capabilities and signal processing on a single die [12], it is a major building block toward the realization of responsive energy-efficient facades.

The capabilities of feature extraction and motion tracking are important for the proposed responsive building facade application [13]. Various motion tracking methodologies have been reported in the literature, which can be classified into four groups: 1) temporal difference based method, which calculates the changes of the pixel intensities in the continuous frames [13]–[20]; 2) correlation-based method, which calculates the product of local pixel intensity and the delayed intensity at the neighboring location [21]; 3) gradient-based method, which calculates the ratio or difference between neighboring pixels [22]–[24]; 4) feature-based method, which extracts and tracks particular features, such as edges or zero-crossings [25]. The tracking results can be further used or combined to do cluster analysis [15], [26] or region-of-interest (ROI) detection [18]. Different schemes are designed depending on the readout methods used for the tracking, such as: 1) global shutter read-out, which uses single exposure and usually requires on-chip memory [27], [28]; 2) rolling shutter read-out, which resets and reads out each pixel in a zig-zag sequence [16], [29]; 3) column-based parallel read-out, which outputs results in parallel [17], [18]; 4) address event representation (AER) read-out, which encodes light intensity in time domain by recording pixel event addresses in sequence [19], [24], [30].

Among the different methodologies, temporal difference based motion tracking algorithm enables higher efficiency and lower complexity as compared to the other methodologies, making it suitable for the implementation in a distributed sensor node. Temporal difference evaluation has been reported in one-way threshold circuit [31] and dual-way threshold circuits [13]–[19]. Single threshold can be implemented in a relative simple circuit, however, dual-threshold temporal difference evaluation method provides higher robustness and

Manuscript received August 27, 2013; revised December 05, 2013 and January 22, 2014; accepted February 04, 2014. Date of publication April 08, 2014; date of current version August 26, 2014. This work was supported in part by the National Science Foundation under Grant EFRI-1038215. This paper was recommended by Associate Editor T. S. Gotarredona. *(Corresponding author: M. Zhang.)*

The authors are with the Department of Electrical and Systems Engineering, The University of Pennsylvania, Philadelphia, PA 19104 USA (e-mail: zhangmilin@seas.upenn.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2014.2312474

accuracy in motion detection. Dual-threshold temporal intensity comparison implemented in global [15], [16], column [17], [18], and pixel-level [14] have been reported in the literature. Global/column level dual-threshold comparator consumes extra power during pixel selection and readout operation phases. Extra noise will be introduced due to the routing of the analog data bus. In addition, the frame rate will be limited and distortion will be introduced for fast moving objects, which makes it not suitable for many motion detection algorithms' implementation. On the other hand, pixel-level dual-threshold comparator have been employed for low-power temporal difference based motion detection algorithm in literature. Traditional dual-way thresholds comparison implemented using two single-end comparators in parallel or in series usually occupies too much area, making it not suitable for pixel-level implementation. Paper [14] reports a minimal pixel-level circuit realizing part of a comparator. However, the timing is complicated due to the comparison with positive and negative thresholds in sequence. This work presents a four pixel motion detection unit, implementing full-functional dual-threshold comparison in the pixel level. The proposed design can be used for various on-chip motion detection algorithms. The power consumption can be minimized due to its simple operation and the short computation time.

In the proposed design, all the reported methods are designed based on the read-out of motion detection results in a 2-D image array. In a CIS with focal plane processing, the peripheral circuits including read-out control, signal digitization, and I/Os, usually dominate the power consumption of the entire chip instead of the active pixels [32]. In 2-D read-out-based motion detection sensors, the power dissipation of the read-out and post-read-out processing increase significantly with frame rate and resolution. In this paper, an energy-optimized, temporal difference based motion tracking algorithm is proposed to solve this problem by extracting motion information from row/column-based processing. A 1-D read-out and a post-read-out processing algorithm are employed. A sub nW motion detection unit is implemented in a pixel-level circuit. Switched-capacitor circuit, analog memory, and dual-threshold comparator are employed, which consume no quiescent power dissipation except for the photon integration during the exposure phase. A global shutter is employed to achieve high-speed object detection without distortion. Compressive video acquisition based on ROI is also realized in this design. The ROIs are highlighted according to the motion detection results.

In addition to image sensing, temperature sensing, which measures local thermal energy and/or radiation on a building facade is implemented on the die. Diodes or bipolar transistors, and parasitic bipolar substrate transistors [33] are widely used in solid-state temperature sensor design to realize the proportional-to-absolute temperature (PTAT) sensing requirement [34]. In this paper, a compact, low-power temperature sensor is implemented using CMOS transistors biased in the weak-inversion region [35]. Multiple analog-to-digital convertors (ADCs), including a 4 Mbps 12-bit pipeline ADC, a 10-bit low-power monotonic slope ADC, and two 1-bit ADC implemented using comparators, have been integrated to allow optimized high-efficiency data conversion. The digital read-outs are used to control of the responsive material employed in the electronic facades.

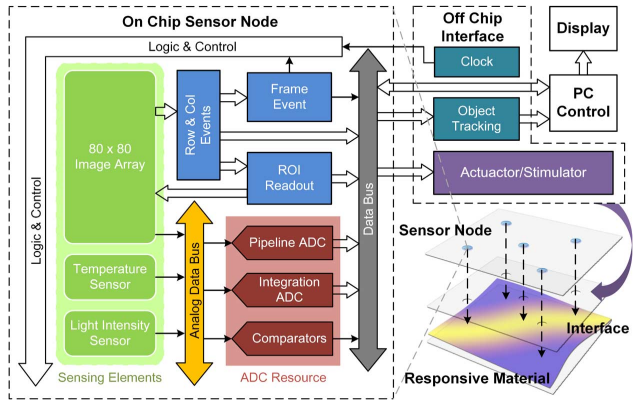


Fig. 1. System block diagram of the multifunctional sensor node with an interface to the responsive material. The sensor node integrates sensing circuits, motion event generation circuits, multiple ADCs and peripheral circuits. The object tracking algorithm is implemented in an off-chip FPGA, realizing compressive image acquisition and control of the responsive material.

The paper is organized as follows. Section II presents an overview of the entire system. Section III proposes the power efficiency optimized motion detection algorithm and ROI-based compressed video output. Section IV details the system architecture, circuit implementation and simulation results. The experimental results and analysis are shown in Section V, while Section VI concludes the paper.

II. System Overview

Fig. 1 illustrates the block diagram of the entire system. The system includes the multifunctional CMOS sensor node with an off-chip interface to the electronic facade. The sensor node integrates sensing circuits, motion event generation circuits, ADC resources, and peripheral logic and control circuits. The object tracking algorithm is implemented in an off-chip FPGA, including digital filtering, compressive image acquisition, and control of the responsive material.

The sensing circuits include a light intensity sensor, a temperature sensor, and an image array with integrated motion detection. A reverse biased PN junction using P-substrate and N-well is employed as the photodetector for the light intensity sensing. Amplifier and correlated double sampling read-out are used to reduce noise. A compact low-power temperature sensor [36] is implemented in the system. An optimized combination of MOSFETs biased at weak-inversion region, linear region, and saturation region are employed in the circuit without resistors. A start-up circuit is integrated to guarantee the circuit settles at the right operating point. All ADC resources are accessible for all analog signals from the sensing circuits via an analog data bus. Both the outputs of the light intensity sensor and temperature sensor are compared with user-defined thresholds by default. The refresh rates, thresholds, and ADC (comparators) clock frequencies can be configured. A 1-bit alarm will be generated according to the comparison results between the captured feature and the user-defined thresholds. One of the ADCs can be triggered for accurate read-out once an alarm is generated.

The on-chip image array has various operation modes: i) event generation mode, which generates 1-bit Frame-Event (FE) signal once a motion or a flashing happens in the focal plane; ii) motion tracking mode, which tracks a moving object based on temporal changes in the focal plane; and iii) video

acquisition mode, which is capable of capturing continuous frames at full-resolution or in the ROI only. Video output mode can be set to wake up when triggered by the FE signal in the event generation mode. The ROI is tracked based on a proposed strategy. Higher refresh rate is employed for the ROIs than for the background in video acquisition mode. The on-chip off-array pipeline ADC is employed for the digitization of the intensity read-out in the video acquisition mode. The details of the image sensor design are presented in the following section.

III. Design of the Multimode Image Sensor

A. Throughput-Based Power Efficiency Optimization

Assume I_{t_k} is the intensity matrix of the frame captured at $t = t_k$, and $I_{t_{k-1}}$ is the one captured at $t = t_{k-1}$. The differential image is calculated as

$$\Delta I_{t_{k,k-1}} = \left| I_{t_k} - I_{t_{k-1}} \right| \tag{1}$$

Pixel-event E_p is defined as

$$E_p(i,j) = \begin{cases} 1 & \text{when } \Delta I_{t_{k,k-1}}(i,j) \geq \xi \\ 0 & \text{when } \Delta I_{t_{k,k-1}}(i,j) < \xi \end{cases} \tag{2}$$

where (i, j) are the coordinates of the pixel, ξ is a threshold value depending on the noise level.

The workload of traditional motion detection methods usually consists of: i) focal plane pixel event generating; ii) pixel events read-out; and iii) post-read-out processing. The total power consumption can be evaluated as

$$P_{pxl-based} = P_{array} + P_{readout} + P_{proc} \tag{3}$$

where P_{array}, $P_{readout}$, and P_{proc} represent the power consumption for generating pixel events in the focal plane processing units, reading out pixel events, and the algorithm's processing on the pixel events, respectively. Given a pixel array with a resolution of $n \times n$, the P_{array} is proportional to the number of pixels n^2. In CMOS image sensor design, shift register (SR) chains are widely used for pixel selection and readout. $P_{readout}$ depends on N_{pxl-rd}, the total number of times the D flip-flops (DFF) in the SR chains are triggered to flip while reading out one frame in a rolling shutter sequence

$$\begin{aligned} N_{pxl-rd} &= \underbrace{(1 + 2(n-2) + 1)}_{Column\ SR's\ flips} \cdot n + \underbrace{(1 + 2(n-2) + 1)}_{Row\ SR's\ flips} \\ &= 2n^2 - 2. \end{aligned} \tag{4}$$

P_{proc} is proportional to the readout pixel events, with a coefficient K_c, which represents the complexity of the processing algorithm. The total power for pixel-event readout can be approximately modeled as

$$P_{pxl-based} = n^2 f_r P_{pxl} + (2n^2 - 2) f_r P_{\mathrm{DFF}} + K_c n^2 f_r P_{\mathrm{DFF}} \tag{5}$$

where f_r is the frame rate. According to (5), the power consumption of the traditional methods is proportional to $n^2 f_r$, so the total power consumption increases dramatically while higher throughput is employed.

In this work, in order to increase motion detection's power efficiency, a row/column-based readout method is proposed. In the proposed algorithm, row-event E_r and column-event E_c are introduced, where

$$E_r(i) = \begin{cases} 1 & \sum_{j=1}^{n} E_p(i,j) > 0 \\ 0 & \sum_{j=1}^{n} E_p(i,j) = 0 \end{cases} \tag{6}$$

$$E_c(j) = \begin{cases} 1 & \sum_{i=1}^{n} E_p(i,j) > 0 \\ 0 & \sum_{i=1}^{n} E_p(i,j) = 0. \end{cases} \tag{7}$$

The total power consumption can now be evaluated as

$$P_{row-based} = P_{array} + P'_{readout} + P'_{proc} \tag{8}$$

where $P'_{readout}$ and P'_{proc} stand for the power consumption of the row/column-based read-out and the post-read-out processing, respectively. $P'_{readout}$ depends on N_{row-rd}, the total number of times the DFFs in the event buffer chains are triggered to flip while reading out one frame. The $2n$ row and column events are first loaded in the shift register buffers, and then shifted out. In the worst case, where every other row and column has an event, the workload for the readout is

$$\begin{aligned} N_{row-rd} &= \underbrace{\left(\frac{1}{2}n\right)}_{Load} \cdot 2 + \underbrace{[n + (n-1) + (n-2) + \ldots + 1]}_{Shift\ event\ out} \cdot 2 \\ &= n^2 + 2n. \end{aligned} \tag{9}$$

Equation (8) can be further expressed according to the DFF's power as

$$P_{row-based} = n^2 f_r P_{pxl} + (n^2 + 2n) f_r P_{\mathrm{DFF}} + K'_c (2n) f_r P_{\mathrm{DFF}} \tag{10}$$

where K'_c stands for the complexity of the processing algorithms based on the row/column events. In an image sensor, the throughput of an $N \times N$ image sensor can be written as

$$\text{Throughput} = N^2 \times F_R \tag{11}$$

where F_R stands for the required frame rate of the image sensor. While the throughput is increasing, the high-speed digital read-out circuits and post-read-out processing circuits become the most power-hungry units, which dominate the total power of the entire sensor. Fig. 2 illustrates a comparison between the pixel-event-based and the proposed row/column-event-based methods, under a same readout workload. A moving tennis ball is captured in the video stream. In Fig. 2(a), an image array with a resolution of 10 × 10 using the pixel-event-based method is employed for the motion detection. The throughput of this imager is 100 events per frame. The detection result is shown in Fig. 2(b), and the ROI readout is shown in Fig. 2(c), where the object's contour is blurred due to the low resolution. On the other hand, an image array with a resolution of 50 × 50 using the proposed row/column-event-based method features the same 100 events output, as shown in Fig. 2(d). The detection result and ROI readout are shown in Fig. 2(e) and (f), respectively, where the size and position of the target are better presented. In addition, the output row/column event addresses can be directly used for ROI window readout.

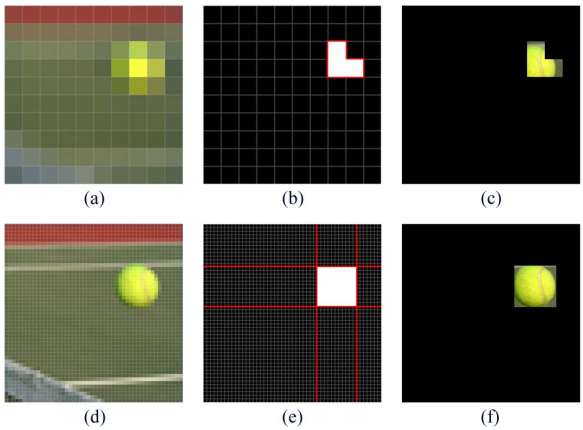


Fig. 2. Comparison between (a)–(c) the object detection using pixel-event-based or (d), (e) row/coloumn-event-based algorithms. A moving tennis ball is captured in the stream. Panel (a) shows the raw frame captured with a resolution of 10×10. Panel (b) shows the detected moving object using the pixel-based detection algorithm featuring a readout workload of 100 events. Panel (c) shows the corresponding ROI readout. Panel (d) shows captured frame with a resolution of 50×50. Panel (e) Shows the detected moving object using the proposed row/column-event-based algorithm featuring a same readout workload of 100 events, panel (f) shows the ROI readout, where object's size and location are better presented.

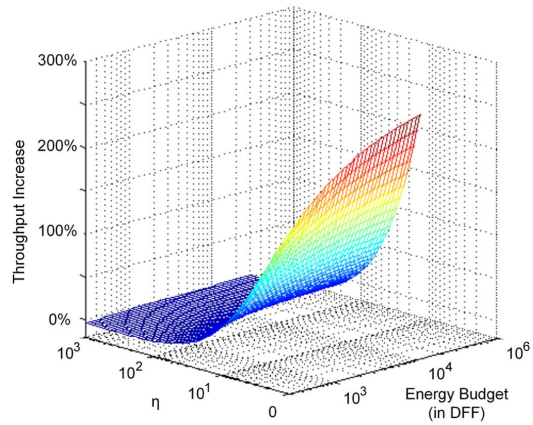


Fig. 3. Numerical analysis of the increase of the throughput of the row/column-based method compared to the pixel-event-based method. The throughputs of the two methods are calculated based on the proposed power model with η and the total power budget as the independent variables. The complexity of the post-processing is assumed to be the same, $K_c = K_c' = 10$. The energy consumption is computed based on the power of a DFF in one clock cycle to avoid the variation with different CMOS technologies.

In order to quantitatively evaluate the improvement of the power efficiency of the proposed algorithm, a numerical analysis of the maximum achievable throughput is employed for the comparison between a pixel-based and a row/column-based motion detection algorithm with the same power budget. Define $\eta = P_{pxl}/P_{DFF}$, which is an evaluation parameter in the focal plane processing circuit. The throughput for the pixel-event-based method and the row/column event-based method is evaluated with η and the total power budget as the independent variables. The increase of the throughput of the row/column-event-based method over the pixel-event-based method is calculated based on (5) and (10). The result is plotted in Fig. 3. Given a limited energy budget, the row/column-event-based method could increase the throughput by more than 200%, which shows a clear advantage in applications which require high efficiency and low pixel level processing power (small η). The analysis shows insights on the trade-off of throughput and detection methods, which provides a way to choose from different detection methods based on the throughput specification, energy budget, and the design specification of the pixel-level processing circuit.

B. Event Generation Mode

A Frame-Event (FE) is generated when pixel-events take place in a majority of pixels in two consecutive image frames. Thus, in an $n \times n$ array, a Frame-Event evaluated according to the statistics of the pixel events, FE_{pxl}, is defined as

$$\mathrm{FE}_{pxl} = \begin{cases} 1 & \text{when } \sum_{j=1}^{n}\sum_{i=1}^{n} E_p(i,j) \geq \alpha \cdot n^2 \\ 0 & \text{when } \sum_{j=1}^{n}\sum_{i=1}^{n} E_p(i,j) < \alpha \cdot n^2 \end{cases} \tag{12}$$

where α is a threshold for the sum of pixel-events within one frame. A 1-bit Frame-Event is widely used as motion trigger. However, as defined in (12), the statistical workload for one frame event is $O(n^2)$. An alternative way to generate a Frame-Event (FE_{row}) is to employ the statistical results of the row and column-events.

$$\mathrm{FE}_{row} = \begin{cases} 1 & \text{when } \sum_{i=1}^{n} E_r(i) + \sum_{j=1}^{n} E_c(j) \geq 2\alpha' n \\ 0 & \text{when } \sum_{i=1}^{n} E_r(i) + \sum_{j=1}^{n} E_c(j) < 2\alpha' n \end{cases} \tag{13}$$

where α' is the threshold for the statistical processing of row and column-events. Using the statistics of the row and column events (FE_{row}) instead of the pixel events (FE_{pxl}) will reduce the workload to $O(n)$ without sacrificing too much accuracy. Image capture will be triggered once a frame event is detected.

C. Motion Tracking Mode

The proposed row- and column-events-based motion tracking algorithm is illustrated in Fig. 4. The four circles on the image array represent one moving object in four consecutive frames. The boxed region shows how a motion region is detected. As the object moves, the temporal intensity changes in the focal plane generate row and column-events E_r and E_c, respectively. Set R_{t_k} and C_{t_k} are row and column event regions which contains rows/columns for which $E_{r_k}(i)/E_{c_k}(j)$ equals 1, respectively. However, the sets R_{t_k} and C_{t_k} are not always continuous within the real object region in practice, especially when the object and the background are of a similar intensity. Thus a single object may cause several motion regions. Gaussian smooth filtering is introduced to perform preprocessing on E_{r_k} and E_{c_k}. The Gaussian smooth filter modifies the input signal by a convolution with a Gaussian function, which is widely used to reduce image noise. The expression of a 1-D filter is given by

$$g(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{x^2}{2\sigma^2}} \tag{14}$$

where σ is the standard deviation. In this paper, we employ it to filter out the sets of row and column-events, resulting in E'_{r_k} and E'_{c_k}. The detected motion region is

$$D_{t_k} = \left\{(i,j) | E'_{r_k}(i) \cdot E'_{c_k}(j) = 1\right\}. \tag{15}$$

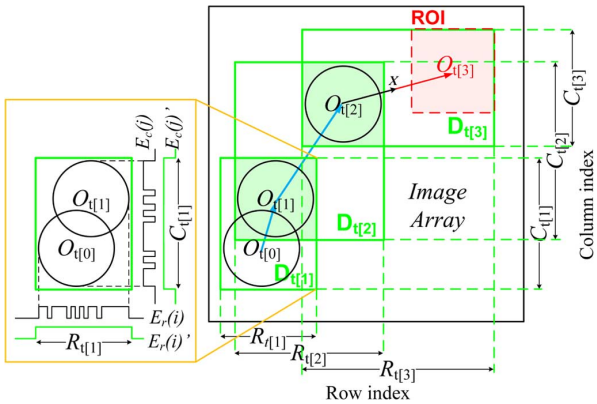


Fig. 4. Illustration of the proposed motion tracking algorithm. Circles on the image array represent the trajectory of one moving object in four consecutive frames from t_0 to t_3. The boxed region shows how the motion region is detected. The object's position at the frame of t_1 is estimated by $D_{t_1} \cap D_{t_2}$. The prediction of ROI at the frame of t_3 is marked by a dashed square.

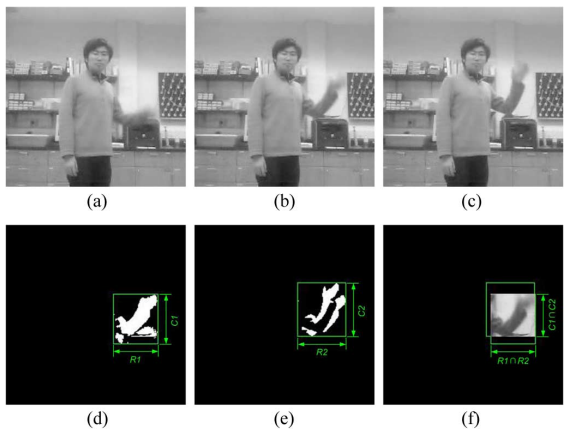


Fig. 5. Simulation result of the proposed motion tracking algorithm. Panels (a)–(c) show the raw frame sequences captured by a normal camera where a person standing still in the scene is waving his arm. Panels (d) and (e) show the pixel-events and the motion region between (a) and (b) and (c) and (d). Panel (f) shows the estimated ROI location.

Eventually, the object in the frame at $t = t_k$ can be determined by

$$\text{Obj}_{t_k} = D_{t_k} \cap D_{t_{k+1}}. \tag{16}$$

Fig. 5 shows a simulation result of this algorithm. Note that the row and column index intersection operation is also very easy to implement in hardware. The intersection address can be directly used for row and column reset/select chain to perform ROI read-out.

Multiple objects in the focal plane can also be detected using this algorithm. In this case, row and/or column event vector E_{r_k}/E_{c_k} contains more than one event region $R_{t_k[1]}, R_{t_k[2]}, \ldots, R_{t_k[n]}/C_{t_k[1]}, C_{t_k[2]}, \ldots, C_{t_k[m]}$. Thus there are mn clusters in D_{t_k} given by

$$D_{t_k[i,j]} = R_{t_k[i]} \cdot C_{t_k[j]} \quad (1 \le i \le n, 1 \le j \le m). \tag{17}$$

It should be noted that $\text{Max}(m, n) \le N \le mn$, where N is the number of real moving objects. Fake objects will be detected in this case. How to identify these "fake" object is discussed in the following section.

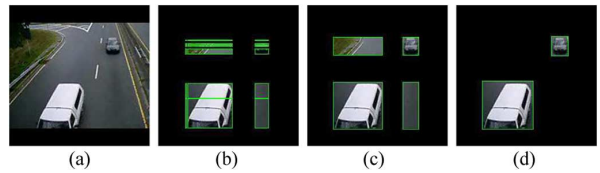


Fig. 6. Simulation of the proposed ROI-based compressive video output mode. (a) The original frame. (b) The motion tracking results before filtering. (c) The motion detection regions after a Gaussian smooth filter is employed, where objects are merged into complete ones. (d) The compressive video output after ROIs evaluated with background.

D. Video Output Mode

The proposed imager enables full-resolution video output as well as compressive video output based on the ROIs. $O_{t_{k-1}}$ is the center of object at the time t_{k-1}, and X_{t_k} is the center of D_{t_k}, as illustrated in Fig. 4. The center of the ROI in the current frame O_{t_k} can be estimated by

$$\overrightarrow{O_{t_{k-1}} O_{t_k}} = 2 \cdot \overrightarrow{O_{t_{k-1}} X_{t_k}}. \tag{18}$$

The size of the ROI is estimated to be the same as the object in the previous frame.

A background modeling is performed off-chip. During the background modeling phase, full resolution images are captured, compared and buffered. After that, only the detected ROI will be read out. The background modeling process will be retriggered once a significant light intensity change is detected from the light sensor.

After the read-out of the ROIs, an evaluation of the ROI is conducted to tell whether it is a real moving object or belongs to the background. A simulation of the ROI-based compressive video output is shown in Fig. 6.

IV. Circuit Implementation

A. Motion Detection Unit

The pixel-level motion detection unit (MDU) enables a 1-bit digital readout of a pixel-event, or an analog readout proportional to the light intensity depending on the selected configuration. The complete circuit for the MDU is shown in Fig. 7.

Four standard active pixel sensors (APS) [37] are integrated within each MDU. There are one photodiode, two reset transistors (M1, M2), one source follower (M3), and switches for the output integrated in a single pixel, as shown in Fig. 7(a). Under intensity acquisition mode, the process begins from a reset phase when both $Row\_rst(i)$ and $Col\_rst(j)$ are low, and the photodiode voltage has been pulled up to V_{DD}. After the reset phase, the photodiode voltage decreases as the photon-generated charges accumulate on the photodiode capacitance. The reset or integration voltages can be readout when the pixel-level switch $Col\_sel(j)$ and row-level switch $Row\_sel(i)$ are turned on. The analog readout will be digitized by the global ADC during the readout phase. Delta-difference sampling is performed off-chip to reduce fixed pattern noise (FPN).

A temporal difference memory, a dual-threshold comparator circuit, and an event generation unit are shared by the four APSs in each MDU. Under motion detection mode, every MDU generates a 1-bit pixel-event E_p as defined in (1) and (2). The MDUs in each row and column will then generate row and column-events E_r and E_c as defined in (6) and (7). The timing

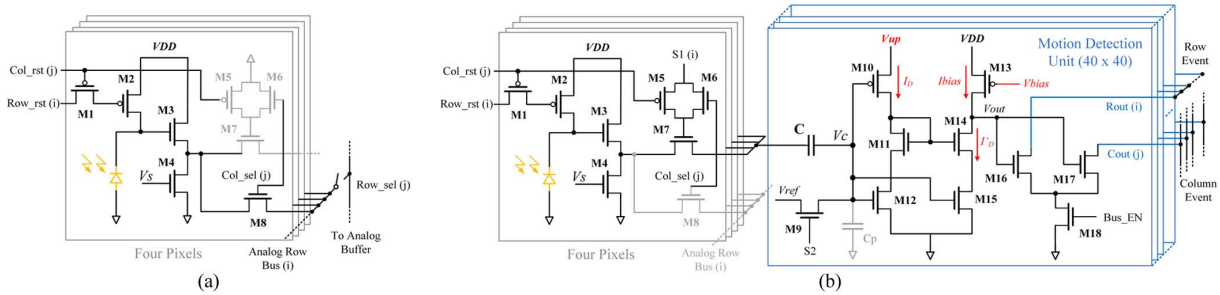


Fig. 7. Complete circuit for the proposed motion detection unit (MDU). A temporal difference memory, a dual-threshold comparator circuit, and event generation circuits are shared by the four APSs in each MDU. (a) Configuration under image acquisition mode. (b) Configuration under motion event generation mode.

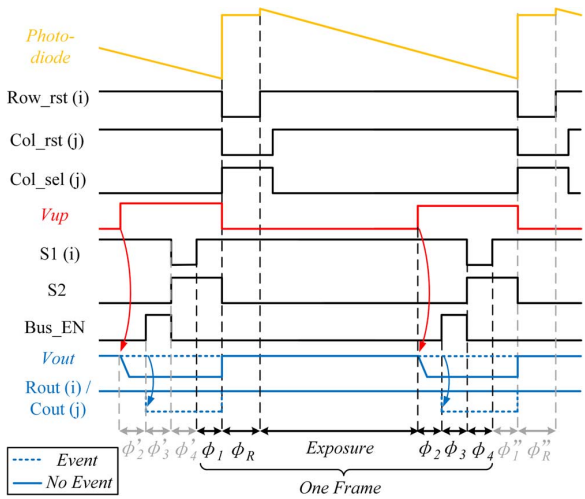


Fig. 8. Timing for a selected motion detection unit (MDU) under motion detection mode.

for the selected pixel in a MDU is shown in Fig. 8. The motion detection process contains six phases in each frame. During $\phi 1$, transmission gate (M5, M6) is turned off, both switches M7 and M9 are on for sampling the integrated voltage $V_{t_{k-1}}$ with respect to the reference voltage

$$Q_1 = C\left(V_{t_{k-1}} - V_{ref}\right) - C_p V_{ref} \tag{19}$$

where C_p is the parasitic capacitor of the input gate. M9 is then turned off in ϕ_R, and the pixel is reset. During $\phi 2$, M7 is turned on, giving

$$Q_2 = C\left(V_{t_k} - V_C\right) - C_p V_C \tag{20}$$

where V_C is the voltage on the input gate of the comparator. According to the law of charge conservation, $Q_1 = Q_2$

$$V_C = \frac{C}{C + C_p}\left(V_{t_k} - V_{t_{k-1}}\right) + V_{ref}. \tag{21}$$

By designing the C so C_p's change with input voltage is neglectable with respect to C, the V_C can be expressed as

$$V_C = \alpha \Delta V_{t_{k-1,k}} + V_{ref} \tag{22}$$

where α is a constant ≈ 1, $\Delta V_{t_{k-1,k}}$ is the difference between two consequent frames.

An inverter-based dual-threshold comparator stage [38] is employed, implemented with M10 and M12. When the input voltage V_C increases from ground to V_{up}, the drain current I_D through M10, M11, and M12 first increases exponentially, then decreases exponentially. M14 and M15 are used to mirror I_D to the output branch in series with a current source M13. The V_{out} depends on the relative current magnitude of the mirrored branch current I'_D and the biasing current I_{bias}. When the input voltage V_C is close to the lower threshold voltage $V_{TH_{dn}}$, M12 should be biased at the subthreshold region. The saturation condition for M12 in the subthreshold region ($V_{DS} > 4\phi_T$) is easy to keep, so the drain current will be dominated by M12

$$I_{Ddn} = \frac{2\mu_n C_{ox}\phi_T^2}{\kappa}\frac{W_{12}}{L_{12}}\exp\frac{-\kappa V_{TN} + \kappa V_C}{\phi_T}. \tag{23}$$

When the input voltage V_C is close to the upper threshold $V_{TH_{up}}$, M10 should be biased in the subthreshold region. The drain current will then be dominated by M10

$$I_{D_{up}} = \frac{2\mu_p C_{ox}\phi_T^2}{\kappa}\frac{W_{10}}{L_{10}}\exp\frac{-\kappa\left(|V_{TP}| + V_C - V_{up}\right)}{\phi_T}. \tag{24}$$

The current source M13 is also biased in the subthreshold region. Thus

$$I_{bias} = \frac{2\mu_p C_{ox}\phi_T^2}{\kappa}\frac{W_{13}}{L_{13}}\exp\frac{-\kappa|V_{TP}| - \kappa(V_{bias} - V_{DD})}{\phi_T}. \tag{25}$$

The lower threshold V_{THdn} is determined by $I_{D_{dn}} = I_{bias}$

$$\begin{aligned} V_{THdn} &= V_{TN} + ln\left(\frac{\mu_p}{\mu_n}\frac{W_{13}}{L_{13}}\frac{L_{12}}{W_{12}}\right)(V_{DD} - V_{bias} - |V_{TP}|) \\ &= A_1 V_{bias} + B_1 \end{aligned} \tag{26}$$

where also A_1 and B_1 are constants by design. The higher threshold $V_{TH_{up}}$ is determined by $I_{D_{up}} = I_{bias}$

$$\begin{aligned} V_{TH_{up}} &= V_{up} - |V_{TP}| - ln\left(\frac{W_{13}}{L_{13}}\frac{L_{10}}{W_{10}}\right)(V_{DD} - V_{bias} - |V_{TP}|) \\ &= A_2 V_{bias} + B_2 + V_{up} \end{aligned} \tag{27}$$

where A_2 and B_2 are constants by design. Equations (26) and (27) show that the two threshold voltages can be controlled by adjusting V_{bias} and V_{up}. Fig. 9 shows a simulation result, while the input V_C increases linearly across the dual-threshold voltages.

Equation (2) is realized in hardware by setting the center voltage of the dual-threshold comparator equal to V_{ref}.

$$V_{ref} = \frac{1}{2}(V_{THup} + V_{THdn}) \tag{28}$$

and the threshold ξ in (2) is

$$\xi = \frac{1}{2}\left(V_{TH_{up}} - V_{TH_{dn}}\right). \tag{29}$$

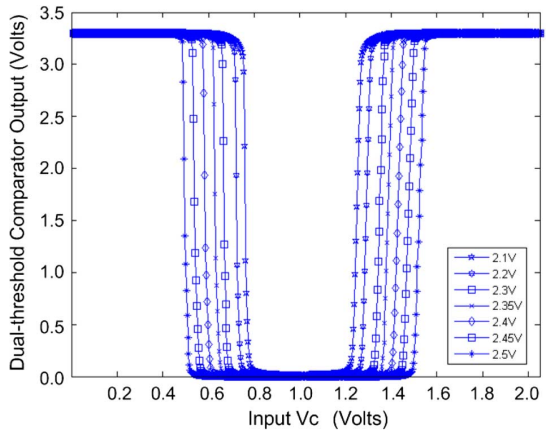


Fig. 9. Simulation results of the output when sweeping the input voltage linearly under different current source biasing.

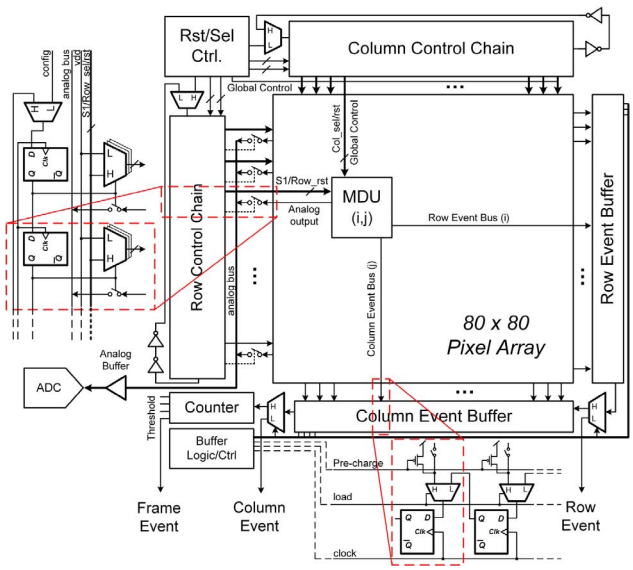


Fig. 10. Architecture of the image sensor. An 80 × 80 pixel array, row and column control chains, row and column event buffers, frame event generator, and peripheral logic and control circuits are integrated.

V_{up} is only turned on during $\phi 2$ to reduce the power consumption. The temporal difference voltage on V_C is compared with a user-defined dual-way thresholds during $\phi 2$. Dynamic logic is further used to generate row and column requests according to (6) and (7). Before $\phi 3$, both row and column request buses are charged to the high level. When Bus_EN signal is valid, V_{out} of the comparator allows M16 and M17 in each block to discharge the buses to a low level in the case of pixel-event detection, or disconnection from the buses. Read-out transistor $M4$ and dual-threshold comparator are only triggered during the readout phase. Thus, there is no quiescent power consumption during the integration phase, which usually takes more than 95% of the operating time during the capture of a single frame. The charges on the capacitor are reset during $\phi 4$.

B. Multimode Image Sensor

The architecture of the multimode image sensor is illustrated in Fig. 10. It integrates an 80 × 80 pixel array, row and column control chains, row and column event buffers, frame event generator, and peripheral logic and control circuits.

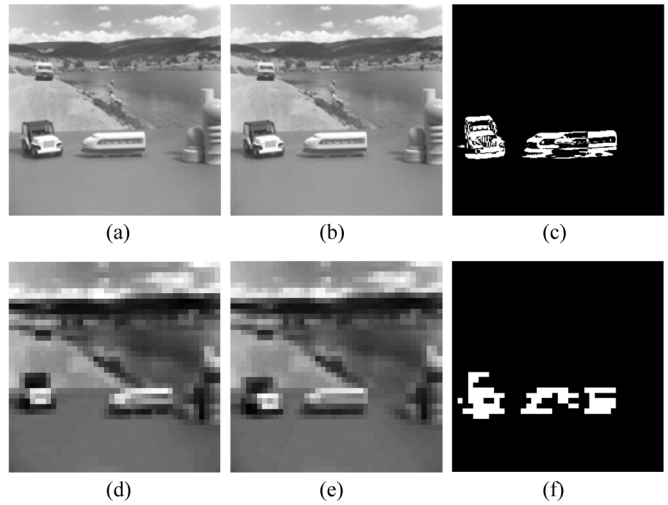


Fig. 11. Circuit-level simulation based on the SPICE models. Panels (a) and (b) show the original image sequences, where two vehicles are moving toward each other. Panel (c) shows the differential image when the threshold is set to be ±15%. Panels (d) and (e) are the magnitudes of the current sources array mapped from the two original image sequences. Panel (f) shows the detection results from the motion detect unit array.

The 80 × 80 pixel array is divided into 2 × 2 pixels' MDUs. The operation mode and timing are controlled by the row and column control chains. Under intensity acquisition mode, a rolling shutter readout sequence is employed. Pixels are selected and reset/readout serially during the readout window. Under the motion detection mode, a global shutter readout is employed. Row and column control chains first select the MDUs to be activated, the control signals are then used to perform motion detection in these MDUs. Row and column event buffers are used to precharge the event buses, and load the results when ready. The event buffers can be configured to send the events to the frame event generator, or output the row and column events for the off-chip processing. Equation (13) is realized in the on-chip global event generator by using a counter with a user-defined threshold. A Gaussian digital filtering is implemented in the FPGA for the off-chip processing.

Fig. 11 shows a circuit-level SPICE simulation. A current source is applied to each photodiode in the pixel array with a current value proportional to the incident light intensity to mimic the photocurrent in each pixel. The value of each current source is updated per frame. The pixel-level MDU consumes 32.18 pJ per frame (33 ms) in the worst case, while the DFF in the given technology and supply voltage consumes 1.48 pJ in one flip. So the η in this design is less than 25.12. The power consumption of the motion detection array is 11 μW in this simulation, at a frame rate of 30 fps and a supply voltage of 3.3 V. The power includes that of the 40 × 40 MDU array, readout circuits, and event output circuits.

C. ADC Design

The analog-to-digital converting unit contains a 12-bit pipeline ADC, a low-power 10-bit monotonic slope ADC and two comparators. The ADCs with different resolution, speed, and power consumption are intentionally designed for different application purposes.

Integrating ADCs have high resolution and good noise rejection, and are ideal for low-bandwidth signals. Fig. 12 shows

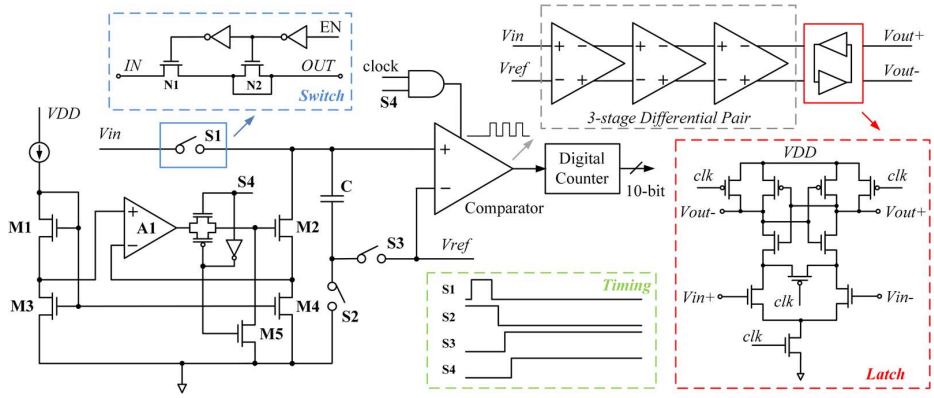


Fig. 12. Circuit schematic and timing of the employed monotonic integrating ADC.

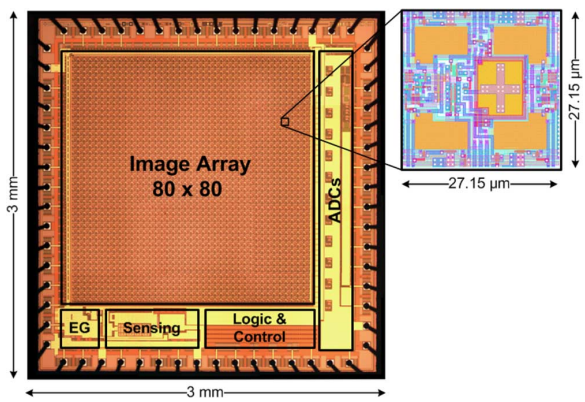


Fig. 13. Microphotograph of the fabricated chip and layout of the motion detection block.

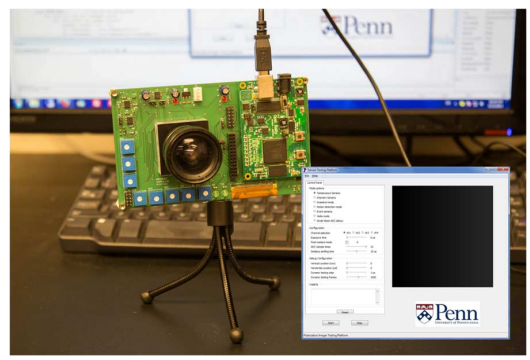


Fig. 14. Photograph of the test bench and a screen shot of the graphic user interface (GUI). The board is designed to integrate the Opal-Kelly FPGA board XEM3010.

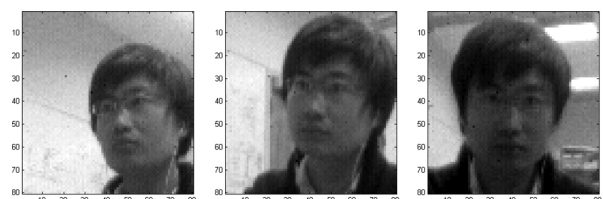


Fig. 15. Video frames captured by the designed imager.

the block diagram and timing of the employed monotonic integrating ADC. It first samples the input voltage on the sampling capacitor, shifts the DC voltage and then discharges the capacitor via a constant current source. The voltage is compared with a reference and the time for the discharging to the reference voltage is proportional to the unknown voltage. A cascaded three-stage preamplifier with a dynamic latch are employed as the comparator. The latch's output is fed into a digital counter when discharging begins. No extra clock is required.

The sample and hold circuit used in this work is also shown in Fig. 12. A dummy switch N2 is employed to reduce charge injection. The width of the switch (N1) is set to be twice the size of the dummy switch (N2). Using three low biasing current differential pairs in cascade as the first stage provides a gain of 30 dB and releases the mismatch problem of the latch. A regulated current source with high output impedance and high compliance voltage range [39] is used as the current source. A shut-off switch (M5) is included to eliminate the current leakage.

V. Experimental Results and Analysis

A prototype chip is implemented in 0.5 μm standard 3M2P CMOS technology, occupying a silicon area of 3×3 mm^2. A microphotograph of the fabricated chip is shown in Fig. 13.

A. Experimental Results

The imaging and motion tracking performance of the chip is tested using an Opal-Kelly XEM3010 FPGA board. The test bench and the designed graphic user interface is shown in Fig. 14. All the digital outputs from the chip are buffered on the SDRAM and then sent to a computer. Fig. 15 shows the video frames captured by the designed sensor node. The resolution employed is 80×80. The performance of the image sensor and the ADC are summarized in Tables I and II, respectively.

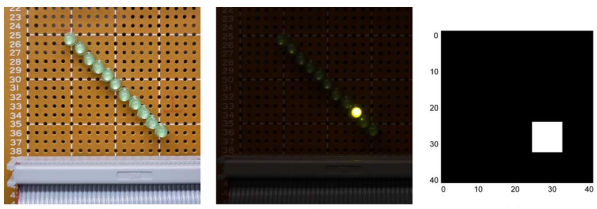
TABLE I
Summary of the Performance of the Multimode Image Sensor

Process Technology	0.5μm 3M2P CMOS
Die Size	3mm $\times$ 3mm
Pixel Array	80 $\times$ 80
Pixel Size	27.15 $\mu m \times$ 27.15 μm
Fill Factor	26.8%
Dynamic Range	48.6 dB
Motion Tracking Power	17 μW

A test board has been made consisting a line of LEDs, as shown in Fig. 16. The LEDs are controlled by the microcontroller individually. A speed controllable motion can be created across the diagonal of the boarding by turning on/off LEDs in

TABLE II
MEASURED PERFORMANCE OF THE MONOTONIC SLOPE ADC

Resolution	10bit
Integral nonlinearity (INL)	< 2.32 LSB
Differential nonlinearity (DNL)	< 2 LSBb
Gain error	$< \pm 1$ %
Signal to noise ratio (SNR)	> 46.39 dB
Input range	$0 \sim 3.3$ V (rail to rail)
Maximum sampling rate	1kHz
Total power consumption	1.74 μW

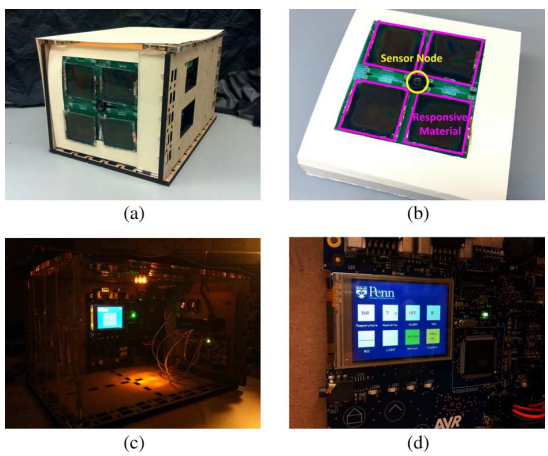


(a) (b) (c)

Fig. 16. Motion detection set-up. (a) LEDs testing board. (b) Motion created by running LEDs. (c) Detected motion region.

TABLE III
SPECIFICATIONS OF THE MEASURED TEMPERATURE SENSOR

Resolution	8.41 mV/°C
Range	-20~80°C
Maximum Errors	+0.50°C/-0.57°C
3-σ Inaccuracy	±0.8°C
Power Consumption	2.95 μW
Area	0.013 mm^2



(a) (b) (c) (d)

Fig. 17. Demonstration of the electronic facade. In (a), a demo setup is built with (b) with one facade covered by four responsive tiles, which are fabricated by filling self-assembled iron oxide colloidal particles in between two ITO glass [10], [11]. The proposed sensor node is located in the middle of the tiles. (c) Inside of the demo house sits the interface board, which contains a microcontroller for driving the material. The LED light's intensity is changed based on the light sensor's detection; seven-segment LEDs are used to display the temperature sensor's output. (d) User panel of the demonstration system.

different sequences. The board is set on the focal plane of the imager. Motion catched in one frame is shown in Fig. 16. The detected motion range is about a width of two LEDs, as expected. The frame rate goes from 10 to 2000 fps. An adaptive algorithm can be further developed for catching moving objects in a broad speed range.

The measured performance of the temperature sensor after a two points calibration is listed in Table III.

B. Demonstration of the Electronic Facade

A prototype setup, as illustrated in Fig. 17, is designed using the proposed multifunctional sensor node and responsive material to demonstrate the concept of an electronic facade. Self-assembled iron oxide colloidal particles [10], [11] are filled in between two ITO glass. The color of the responsive tile can be controlled by the voltage difference applied between the two ITO glass plates. A 32-bit AVR microcontroller is used in the demonstration for the control of the sensor node chip and the responsive material. It also offers a graphic user interface. The material tiles are configured to change according to the different sensing results from the proposed sensor node.

VI. CONCLUSION

In this paper, a low-power multifunctional CMOS sensor node integrating light intensity sensing, temperature sensing, and motion tracking is designed for use in an electronic responsive building facade. Power management is performed at both system and circuit levels. A model for the power dissipation and throughput of motion detection sensors is proposed for the first time, according to which, a hardware-friendly power-efficient optimized motion tracking algorithm is proposed and implemented in the sensor node. The proposed design was fabricated in 0.5 μm 3M2P standard CMOS technology, occupying 3×3 mm^2 silicon area. The total power consumption is 17 μW, while the pixel array performs in the motion detection mode with a frame rate of 30 fps. A prototype is built to demonstrate the concept of an electronic building facade using the proposed sensor node and the customized responsive facade tiles.

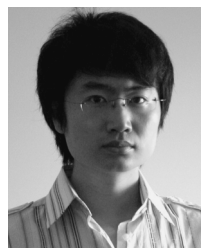
ACKNOWLEDGMENT

The authors would like to thank MOSIS Education Program for fabricating the chip. The authors would also like to thank the cooperation from Dr. S. Yang's research group in the University of Pennsylvania and J. Sabin's studio in Cornell University.

REFERENCES

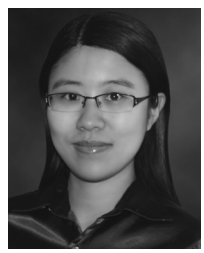
[1] D & R International, Ltd., 2011 Buildings Energy Data Book Buildings Technologies Program Energy Efficiency and Renewable Energy, U.S. Dept. of Energy, Washington, DC, 2012.
[2] Responsive Architecture. Wikipedia [Online]. Available: http://en.wikipedia.org/wiki/Responsive_architecture
[3] Galleria Hall West Seoul, South Korea by UN Studio [Online]. Available: http://www.earchitect.co.uk/korea/galleria_department_store_seoul.htm
[4] Institut Du Monde Arabe by Jean Nouvel [Online]. Available: http://www.greatbuildings.com/buildings/L_Institut_du_Monde_Arabe.html
[5] Aegis Hypo-Surface by deCOi [Online]. Available: http://www.newitalianblood.com/show.pl?id=684
[6] POLA Ginza Building Facade by Nikken Sekkei + Yasuda Atelier [Online]. Available: http://www.adaptivebuildings.com/pola-ginza.html
[7] SmartWrap? By Kieran Timberlake Architects [Online]. Available: http://kierantimberlake.com/research/smartwrap_research_1.html
[8] C. Wang, D. Hwang, Z. Yu, K. Takei, J. Park, T. Chen, B. Ma, and A. Javey, "User-interactive electronic skin for instantaneous pressure visualization," *Nature Mater.*, vol. 12, no. 8, pp. 1–6, Jul. 2013.
[9] M. P. Gutierrez and L. P. Lee, "Multiscale design and integration of sustainable building functions," *Science*, vol. 341, no. 6143, pp. 247–248, Jul. 2013.
[10] H. Wang, Q. W. Chen, Y. B. Sun, and M. Y. He, "Synthesis of superparamagnetic colloidal nanochains as magnetic-responsive Bragg reflectors," *J. Phys. Chem. C*, vol. 114, pp. 19660–19666, 2010.
[11] H. Wang, Q. W. Chen, Y. F. Yu, K. Cheng, and Y. B. Sun, "Size- and solvent-dependent magnetically responsive optical diffraction of carbon-encapsulated superparamagnetic colloidal photonic crystals," *J. Phys. Chem. C*, vol. 115, pp. 11427–11434, 2011.

[12] E. R. Fossum and S. Member, "CMOS image sensors: Electronic camera-on-a-chip," *IEEE Trans. Electron Devices*, vol. 44, no. 10, pp. 1689–1698, Oct. 1997.
[13] X. Liu, M. Zhang, and J. Van der Spiegel, "A low power multi-mode CMOS image sensor with integrated on-chip motion detection," in *IEEE Int. Symp. Circuits Syst.*, May 2013, pp. 2416–2419.
[14] Y. Chi, U. Mallik, and M. Clapp, "CMOS camera with in-pixel temporal change detection and ADC," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2187–2196, 2007.
[15] S. Chen, W. Tang, and E. Culurciello, "A 64 × 64 pixels UWB wireless temporal-difference digital image sensor," *IEEE Trans. Very Large Scale Integration (VLSI) Syst.*, vol. 20, no. 12, pp. 2232–2240, Dec. 2012.
[16] Z. Fu and E. Culurciello, "A 1.2 mW CMOS temporal-difference image sensor for sensor networks," in *Proc. Int. Symp. Circuits Syst.*, 2008, pp. 1064–1067.
[17] H. Nomura and T. Shima, "A 256 × 256 BCAST motion detector with simultaneous video output," in *ISSCC Dig. Tech. Papers*, 1998, pp. 226–227.
[18] J. Choi, S. Park, J. Cho, and E. Yoon, "A 3.4 μW CMOS image sensor with embedded feature-extraction algorithm for motion-triggered object-of-interest imaging," in *ISSCC Dig. Tech. Papers*, 2013, pp. 478–479.
[19] P. Lichtsteiner, C. Posch, and T. Delbruck, "A 128 × 128 120 dB 15 μs latency asynchronous temporal contrast vision sensor," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 566–576, 2008.
[20] G. Kim, M. Barangi, Z. Foo, N. Pinckney, S. Bang, D. Blaauw, and D. Sylvester, "A 467 nW CMOS visual motion sensor with temporal," in *ISSCC Dig. Tech. Papers*, 2013, pp. 480–482.
[21] A. G. Andreou, K. Strohbehn, and R. E. Jenkins, "Silicon retina for motion computation," *Proc. IEEE ISCAS*, vol. 3, pp. 1373–1376, 1991.
[22] R. Etienne-Cummings, J. Van der Spiegel, and P. Mueller, "A focal plane visual motion measurement sensor," *IEEE Trans. Circuits Syst. I: Fund. Theory Appl.*, vol. 44, pp. 55–66, 1997.
[23] N. Massari and M. Gottardi, "A 100 dB dynamic-range CMOS vision sensor with programmable image processing and global feature extraction," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 647–657, Mar. 2007.
[24] M. Gottardi, N. Massari, and S. A. Jawed, "A 100 μW 128 × 64 pixels contrast-based asynchronous binary vision sensor for sensor networks applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1582–1592, May 2009.
[25] H. Jiang and C. Wu, "A 2-D velocity- and direction-selective sensor with BJT-based silicon retina and temporal zero-crossing detector," *IEEE J. Solid-State Circuits*, vol. 34, no. 2, pp. 241–247, Feb. 1999.
[26] B. Zhao, X. Zhang, and S. Chen, "A CMOS image sensor with on-chip motion detection and object localization," *IEEE Trans. Circuits Syst. Video Technol.*, vol. 22, no. 4, pp. 581–588, Apr. 2012.
[27] M. Sakakibara and Y. Oike, "An 83 dB-dynamic-range single-exposure global-shutter CMOS image sensor with in-pixel dual storage," in *ISSCC Dig. Tech. Papers*, 2012, vol. 56, no. 11, pp. 420–421.
[28] Y. Tochigi, K. Hanzawa, Y. Kato, R. Kuroda, H. Mutoh, R. Hirose, H. Tominaga, K. Takubo, Y. Kondo, and S. Sugawa, "A global-shutter CMOS image sensor with readout speed of 1-Tpixel/s burst and 780-Mpixel/s continuous," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 329–338, Jan. 2013.
[29] E. Ringaby and P. Forssen, "Scan rectification for structured light range sensors with rolling shutters," *Proc. IEEE ICCV*, pp. 1575–1582, Nov. 2011.
[30] E. Culurciello, R. Etienne-Cummings, and K. A. Boahen, "A biomorphic digital image sensor," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 281–294, Feb. 2003.
[31] S. Yang, K. Kim, E. Kim, S. Member, K. Baek, S. Kim, and S. Member, "An ultra low power CMOS motion detector," *IEEE Trans. Consumer Electron.*, vol. 55, no. 4, pp. 2425–2430, Nov. 2009.
[32] Y. Oike and A. El Gamal, "CMOS image sensor with per-column $\Sigma\Delta$ ADC and programmable compressed sensing," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 318–328, Jan. 2013.
[33] M. Pertijs, "A CMOS smart temperature sensor with a 3 inaccuracy of $\pm$ 0.1 C from -55°C to 125 °C," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2805–2815, Dec. 2005.
[34] A. Bakker and J. Huijsing, "Micropower CMOS temperature sensor with digital output," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 933–937, Jul. 1996.
[35] E. A. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE J. Solid-State Circuits*, vol. 12, no. 3, pp. 224–234, Jun. 1977.
[36] J. Dantas and H. Costa, "Low-power high-rensponsivity CMOS temperature sensor," *Proc. IEEE Int. Instrumentation and Measurement Technol. Conf.*, pp. 2–6, May 2008.
[37] S. K. Mendis *et al.*, "CMOS active pixel image sensors for highly integrated imaging systems," *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 187–197, Feb. 1997.
[38] S. Mitra and G. Indiveri, "A low-power dual-threshold comparator for neuromorphic systems," *Res. Microelectron. Electron.*, vol. 2, pp. 198–201, 2005.
[39] O. Charlon and W. Redman-White, "Ultra high-compliance CMOS current mirrors for low voltage charge pumps and references," in *Proc. Eur. Solid-State Circuits Conf.*, 2004, pp. 227–230.



Xilin Liu (S'13) received the B.S. degree in electrical engineering from the Harbin Institute of Technology, Harbin, China, in 2011, and the M.S. degree in electrical engineering from the University of Pennsylvania, Philadelphia, PA, USA, in 2013, where he is currently working toward the Ph.D. degree.

His research interests include CMOS image sensors and low-power focal-plane signal processing. He is also interested in mixed-signal integrated circuits design for biomedical microsystems, especially for the brain–computer interface.



Milin Zhang (S'06–M'11) received the B.S. and M.S. degrees in electronic engineering from Tsinghua University, Beijing, China, in 2004 and 2006, respectively, and the Ph.D. degree from the Hong Kong University of Science and Technology, Hong Kong.

She is currently a Postdoctoral Researcher at the University of Pennsylvania. Her research interests include designing of traditional and various nontraditional imaging sensors, such as polarization imaging sensors and focal-plane compressive acquisition image sensors. She is also interested in biomedical sensing applications and new sensor designs.

Jan Van der Spiegel (S'73–M'79–SM'90–F'02) received the Masters degree in electro-mechanical engineering and the Ph.D. degree in electrical engineering from the University of Leuven, Leuven, Belgium, in 1974 and 1979, respectively.

He is currently a Professor and Associate Dean for Education of the Electrical and Systems Engineering Department, and the Director of the Center for Sensor Technologies at the University of Pennsylvania, Philadelphia, PA, USA He is the former chair of the Electrical Engineering and Interim Chair of the Electrical and Systems Engineering Departments. His primary research interests are in mixed-mode VLSI design, CMOS vision sensors for polarization imaging, biologically based image sensors and sensory information processing systems, microsensor technology, and analog-to-digital converters. He is the author of over 160 journal and conference papers and holds 4 patents.

He is a Fellow of the IEEE and the recipient of the IEEE 2007 EAB Major Educational Innovation Award, the IEEE Third Millennium Medal, the UPS Foundation Distinguished Education Chair, and the Bicentennial Class of 1940 Term Chair. He received the Christian and Mary Lindback Foundation, and the S. Reid Warren Award for Distinguished Teaching, and the Presidential Young Investigator Award. He has served on several IEEE program committees (IEDM, ICCD, ISCAS, and ISSCC) and was the Technical Program Chair of the 2007 International Solid-State Circuit Conference (ISSCC 2007). He is an elected member of the IEEE Solid-State Circuits Society and is also the SSCS Chapters Chairs Coordinator and former editor of *North and South America of Sensors and Actuators*. He is a member of Phi Beta Delta and Tau Beta Pi.